ADVANCED TECHNOLOGY

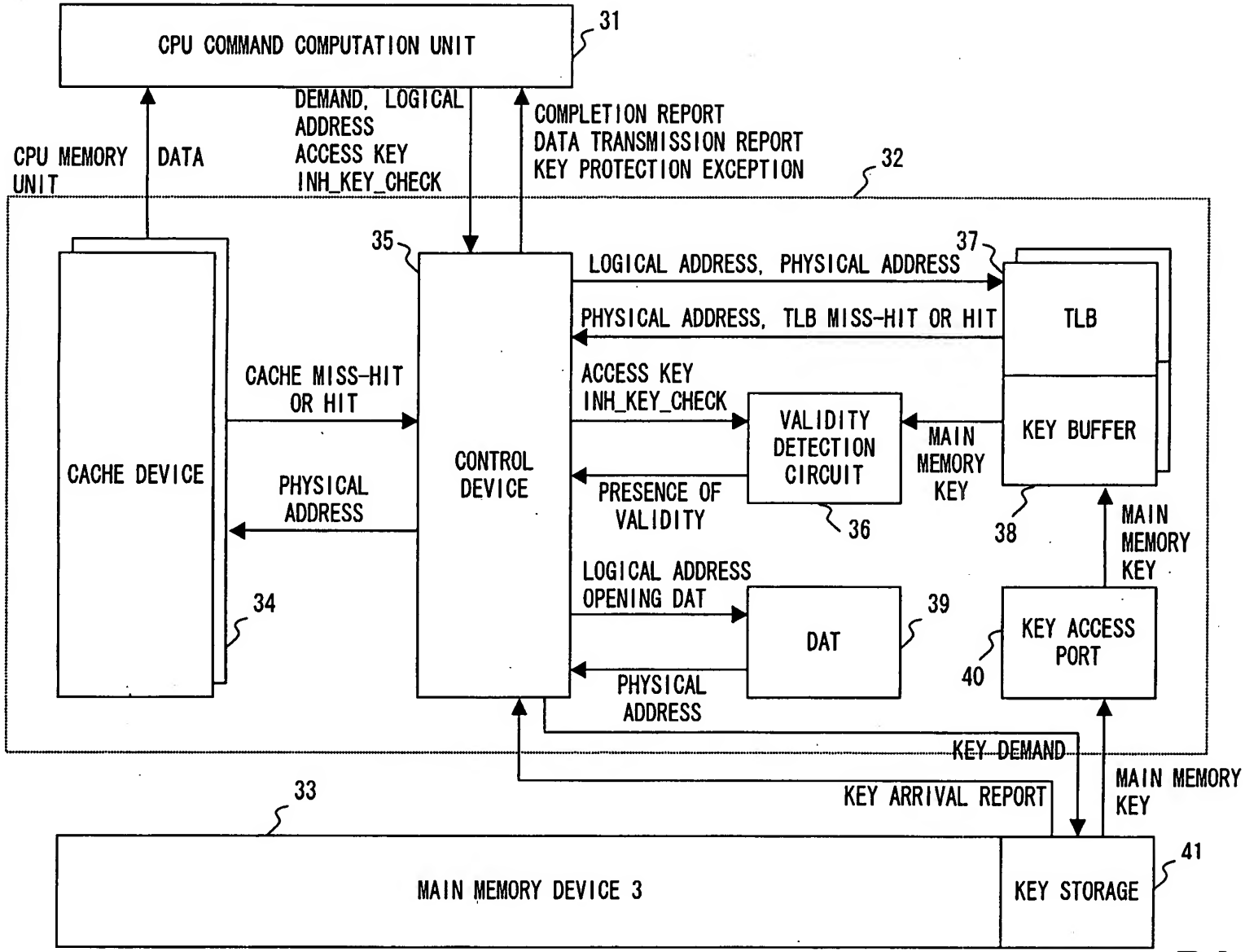


FIG. 1A

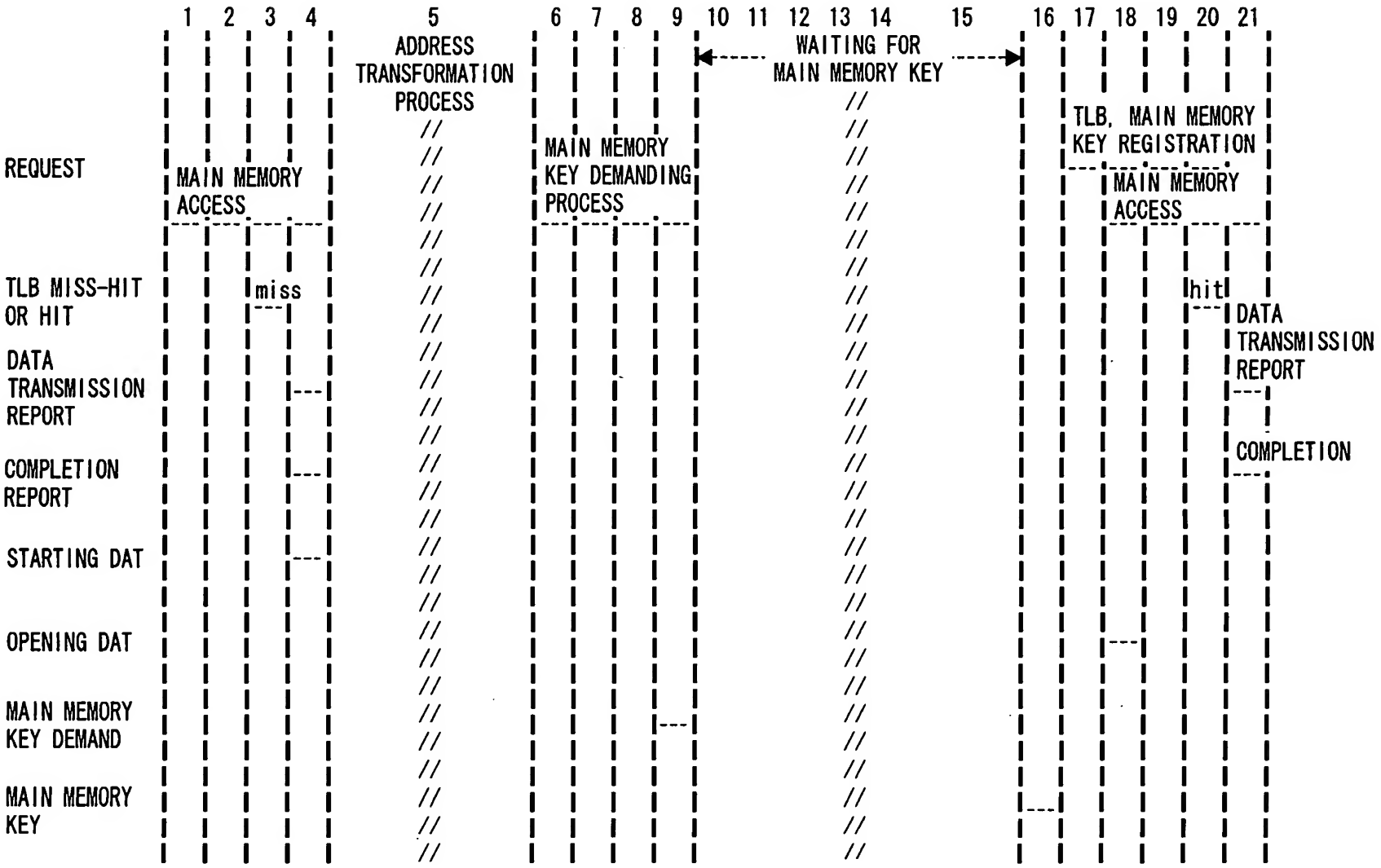

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
REQUEST
MAIN MEMORY ACCESS
ADDRESS TRANSFORMATION PROCESS
MAIN MEMORY KEY DEMANDING PROCESS
WAITING FOR MAIN MEMORY KEY
TLB, MAIN MEMORY KEY REGISTRATION
MAIN MEMORY ACCESS
TLB MISS-HIT OR HIT
miss
hit
DATA TRANSMISSION REPORT
DATA TRANSMISSION REPORT
COMPLETION REPORT
COMPLETION
STARTING DAT
OPENING DAT
MAIN MEMORY KEY DEMAND
MAIN MEMORY KEY

FIG. 1B

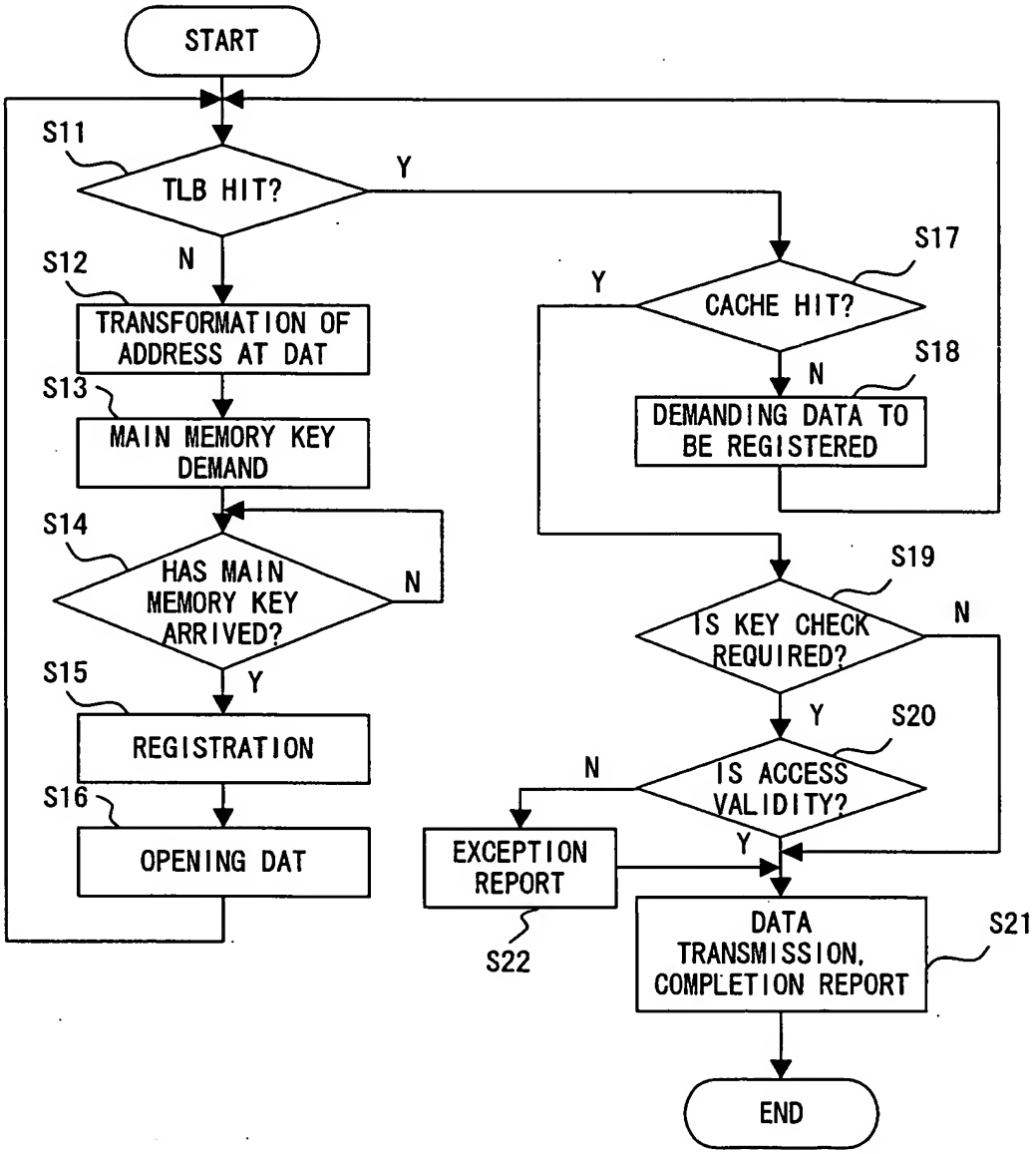

START
S11
TLB HIT?
Y
N
S12
TRANSFORMATION OF ADDRESS AT DAT
S13
MAIN MEMORY KEY DEMAND
S14
HAS MAIN MEMORY KEY ARRIVED?
N
Y
S15
REGISTRATION
S16
OPENING DAT
S17
CACHE HIT?
Y
N
S18
DEMANDING DATA TO BE REGISTERED
S19
IS KEY CHECK REQUIRED?
N
Y
S20
IS ACCESS VALIDITY?
N
Y
EXCEPTION REPORT
S22
DATA TRANSMISSION, COMPLETION REPORT
S21
END

FIG. 1C

EP 2 320 609 A1

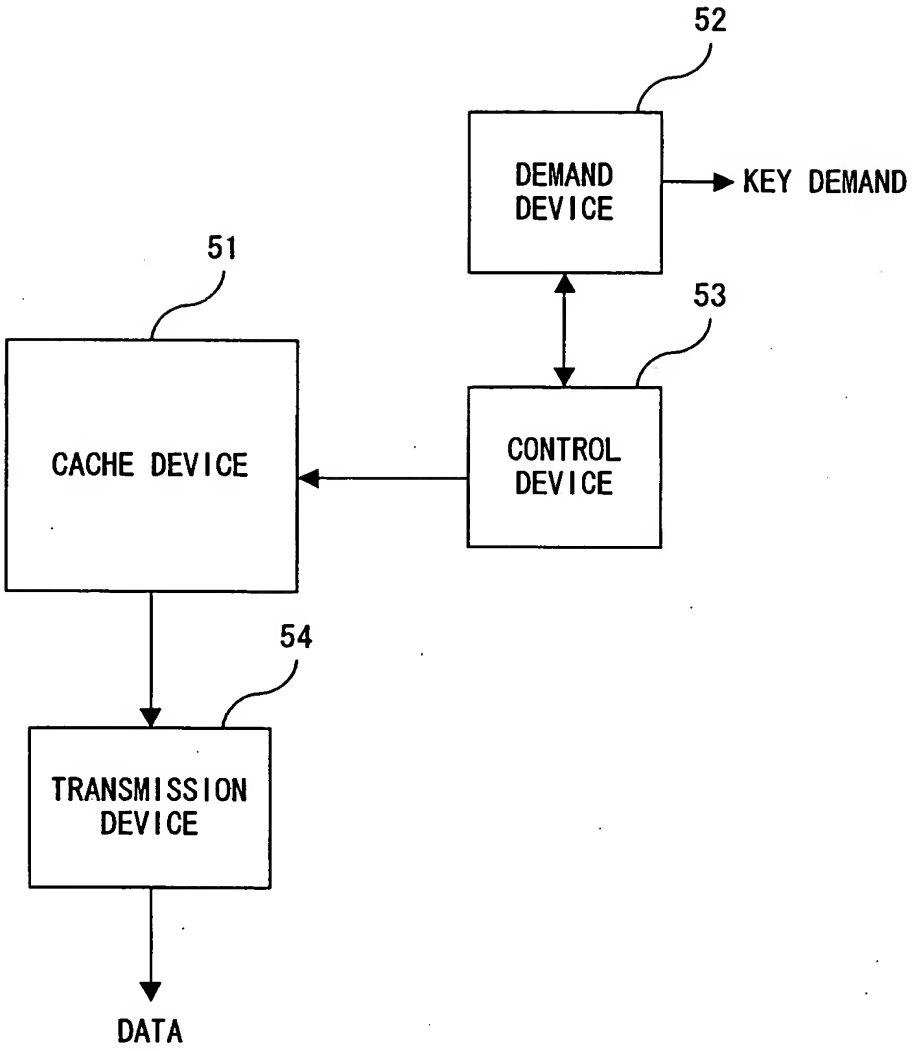


FIG. 2A

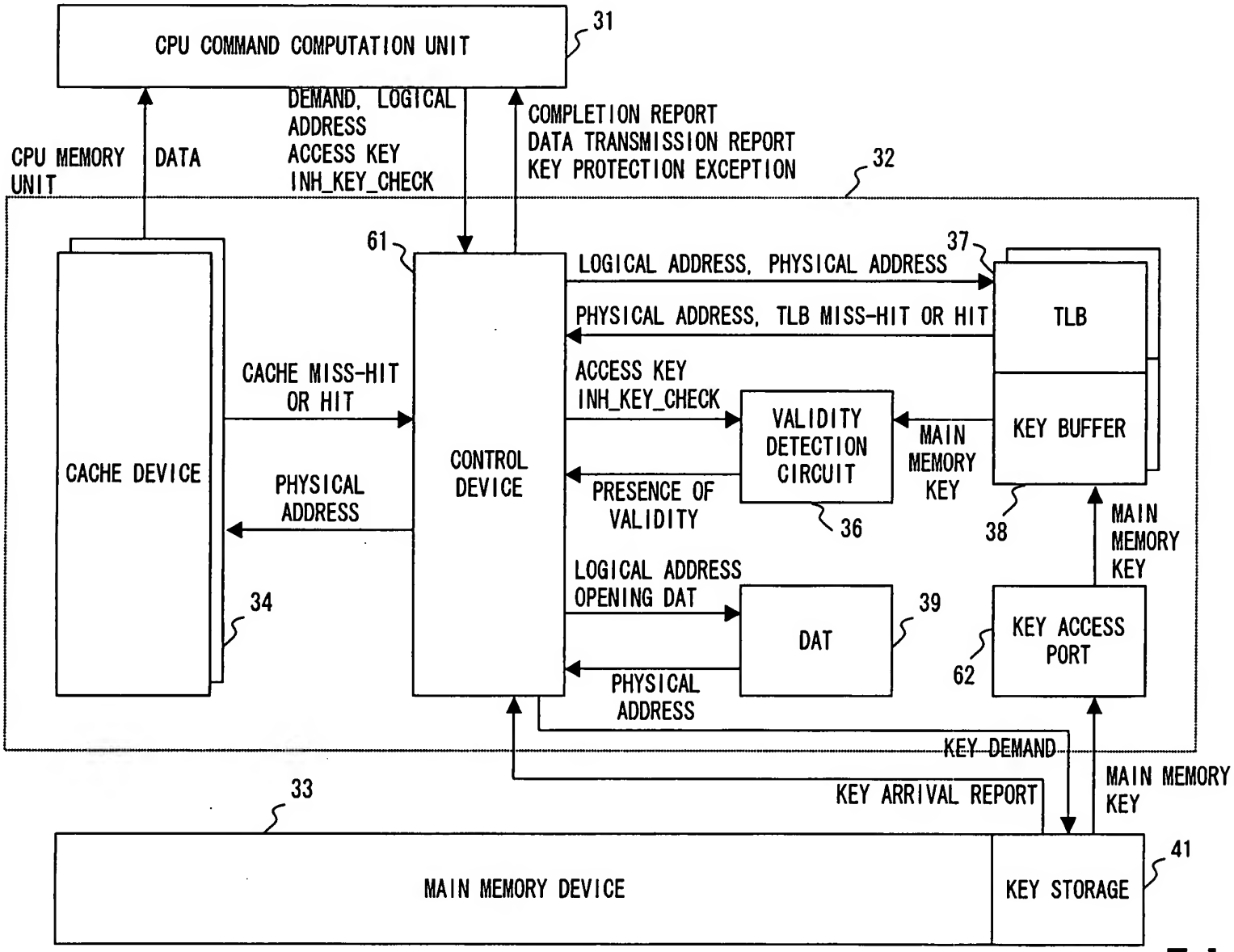

CPU COMMAND COMPUTATION UNIT
31
CPU MEMORY UNIT
DATA
DEMAND, LOGICAL ADDRESS
ACCESS KEY
INH_KEY_CHECK
COMPLETION REPORT
DATA TRANSMISSION REPORT
KEY PROTECTION EXCEPTION
32
61
37
LOGICAL ADDRESS, PHYSICAL ADDRESS
PHYSICAL ADDRESS, TLB MISS-HIT OR HIT
TLB
CACHE MISS-HIT OR HIT
ACCESS KEY
INH_KEY_CHECK
VALIDITY DETECTION CIRCUIT
MAIN MEMORY KEY
KEY BUFFER
CACHE DEVICE
CONTROL DEVICE
PHYSICAL ADDRESS
PRESENCE OF VALIDITY
36
38
MAIN MEMORY KEY
LOGICAL ADDRESS OPENING DAT
34
39
DAT
KEY ACCESS PORT
62
PHYSICAL ADDRESS
KEY DEMAND
MAIN MEMORY KEY
KEY ARRIVAL REPORT
33
MAIN MEMORY DEVICE
KEY STORAGE
41

FIG. 2B

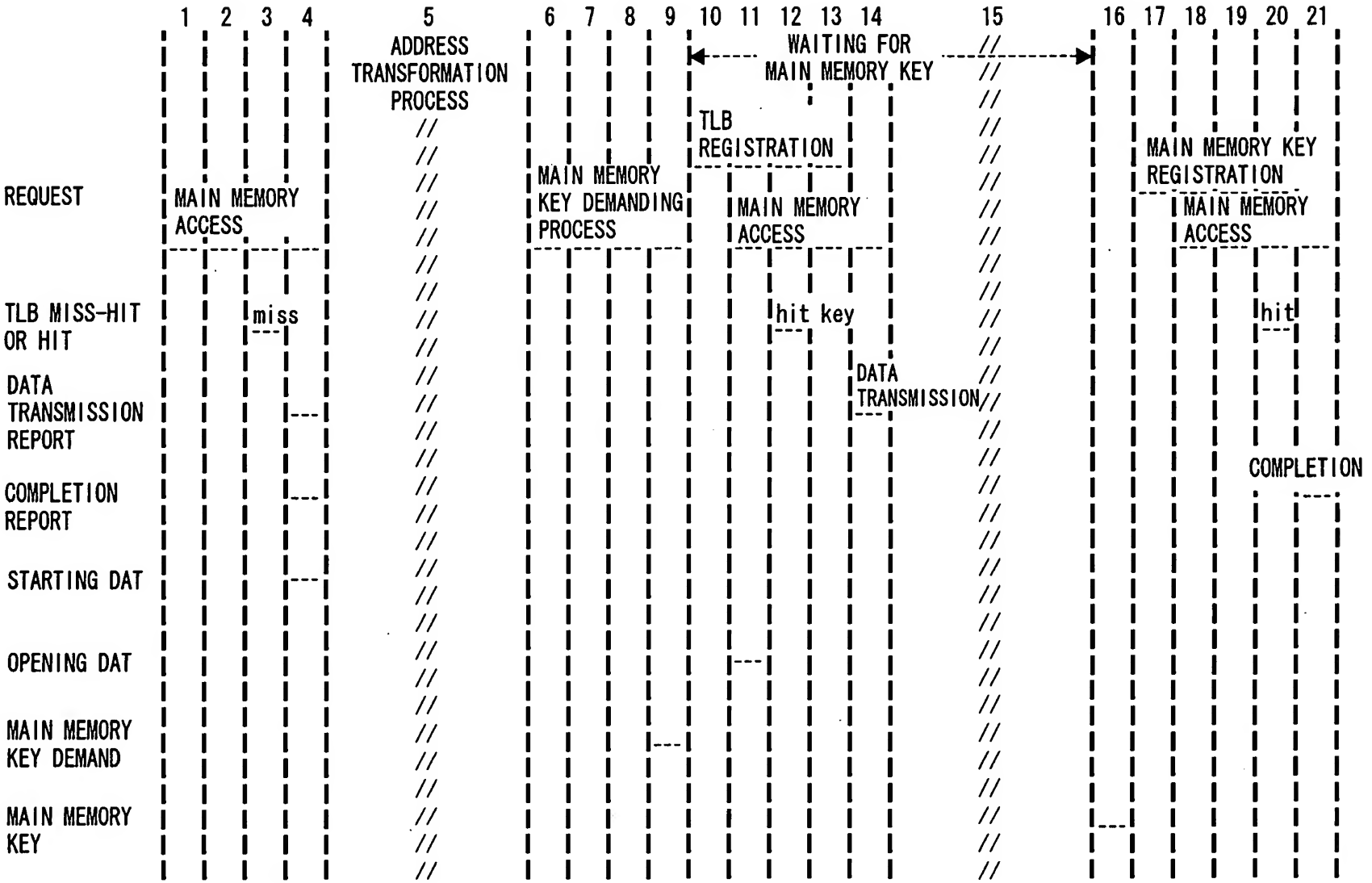

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
REQUEST
MAIN MEMORY ACCESS
ADDRESS TRANSFORMATION PROCESS
WAITING FOR MAIN MEMORY KEY
TLB REGISTRATION
MAIN MEMORY KEY DEMANDING PROCESS
MAIN MEMORY ACCESS
MAIN MEMORY KEY REGISTRATION
MAIN MEMORY ACCESS
TLB MISS-HIT OR HIT
miss
hit key
hit
DATA TRANSMISSION REPORT
DATA TRANSMISSION
COMPLETION REPORT
COMPLETION
STARTING DAT
OPENING DAT
MAIN MEMORY KEY DEMAND
MAIN MEMORY KEY

FIG. 3

20220 T9TE800T

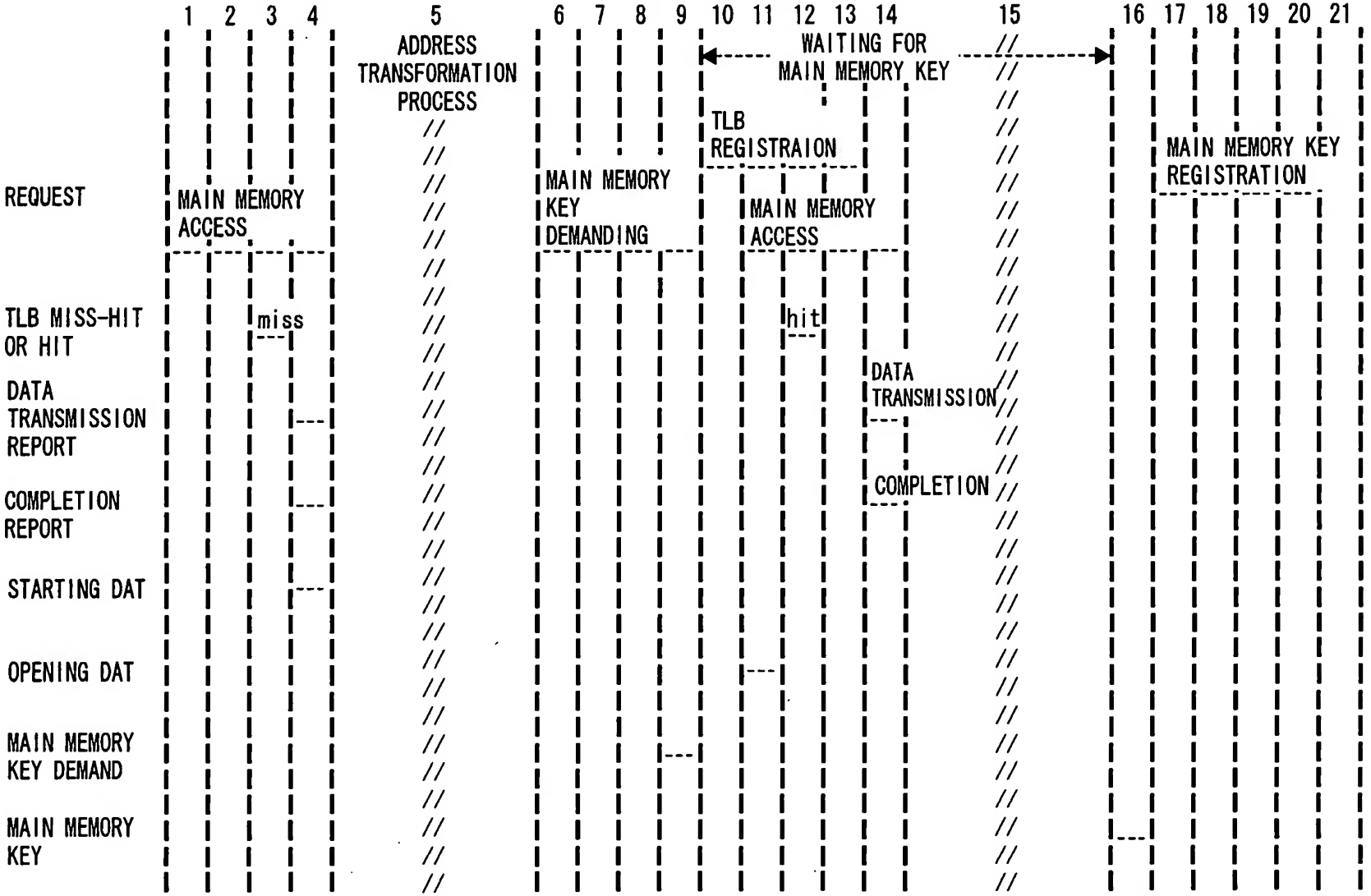


FIG. 4

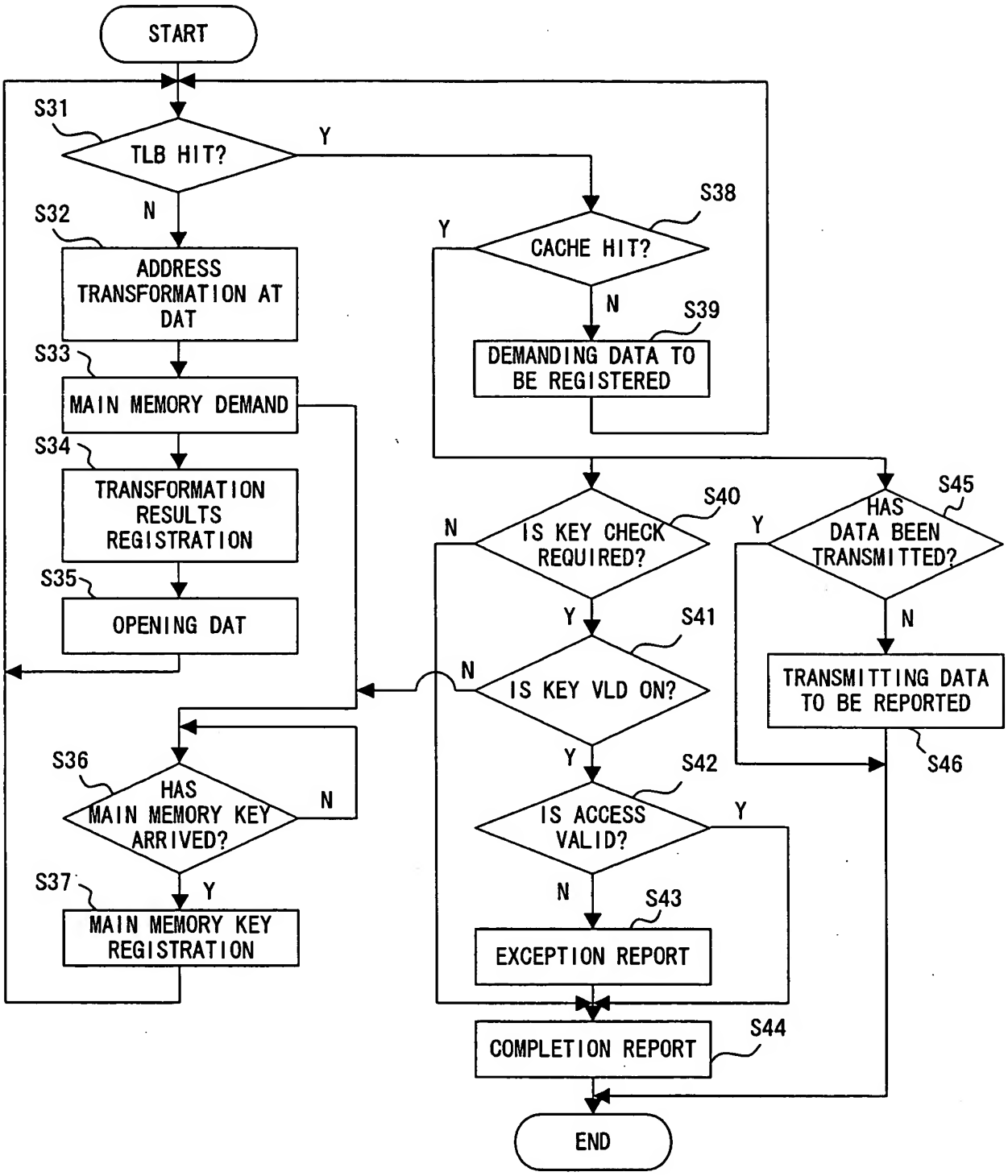

START
S31
TLB HIT?
Y
N
S32
ADDRESS TRANSFORMATION AT DAT
S33
MAIN MEMORY DEMAND
S34
TRANSFORMATION RESULTS REGISTRATION
S35
OPENING DAT
S36
HAS MAIN MEMORY KEY ARRIVED?
N
Y
S37
MAIN MEMORY KEY REGISTRATION
S38
CACHE HIT?
Y
N
S39
DEMANDING DATA TO BE REGISTERED
S40
IS KEY CHECK REQUIRED?
N
Y
S41
IS KEY VLD ON?
N
Y
S42
IS ACCESS VALID?
Y
N
S43
EXCEPTION REPORT
S44
COMPLETION REPORT
S45
HAS DATA BEEN TRANSMITTED?
Y
N
TRANSMITTING DATA TO BE REPORTED
S46
END

FIG. 5

20220 TYPEBOOT

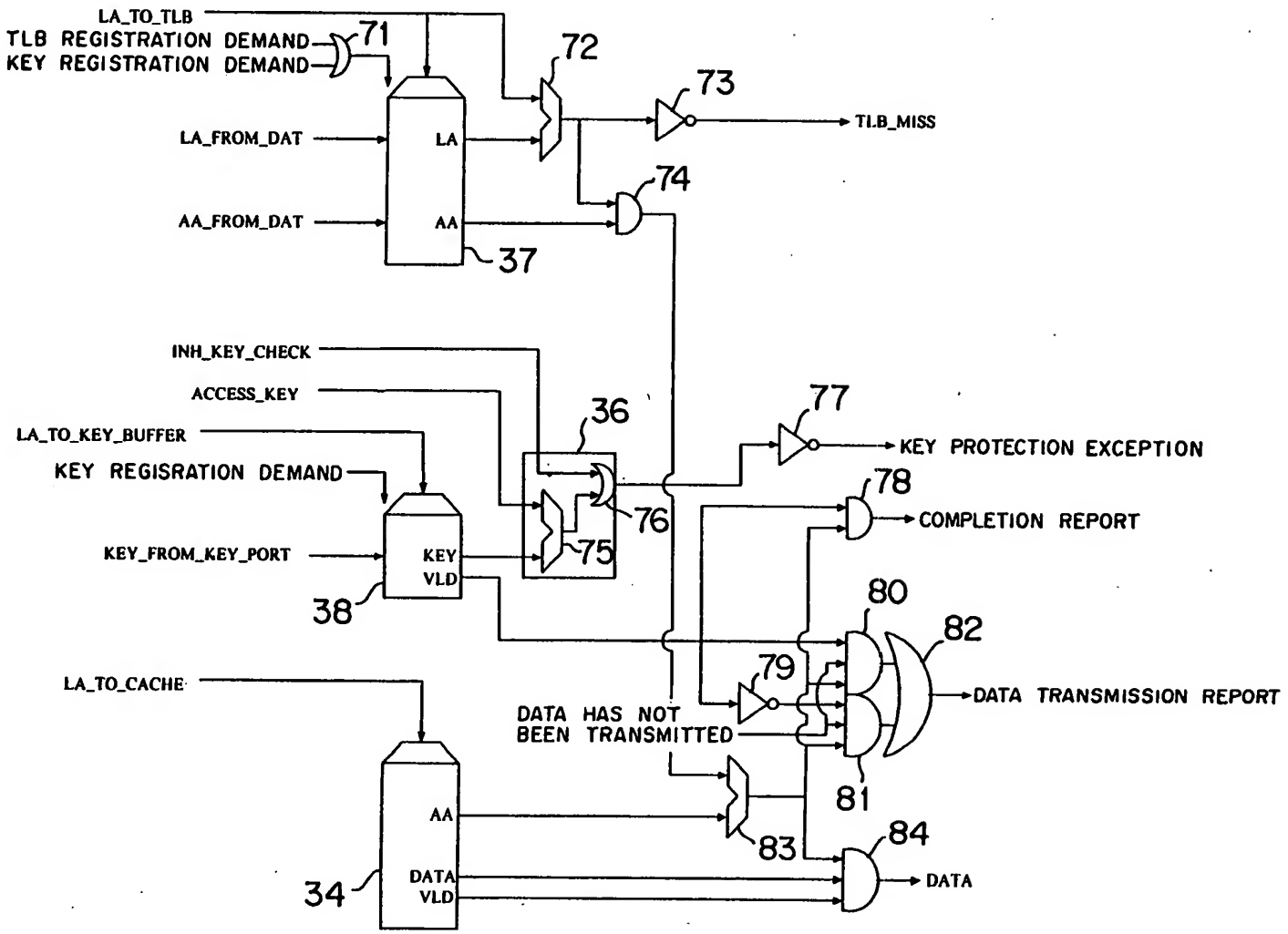


FIG. 6

EP 0 854 430 A2

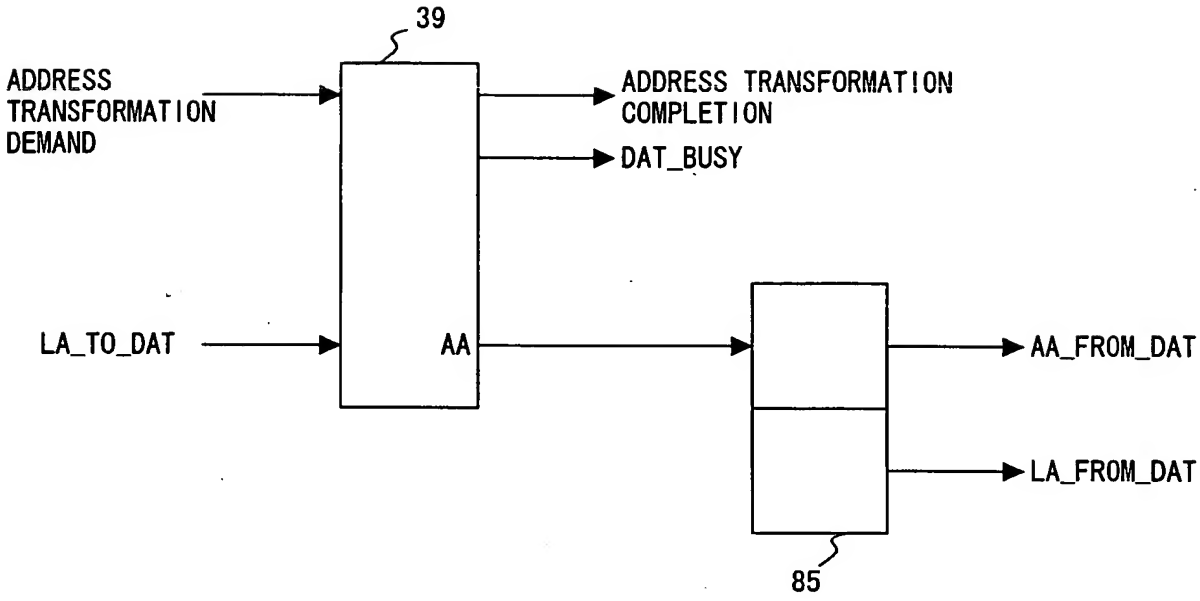


FIG. 7

8520-P8304

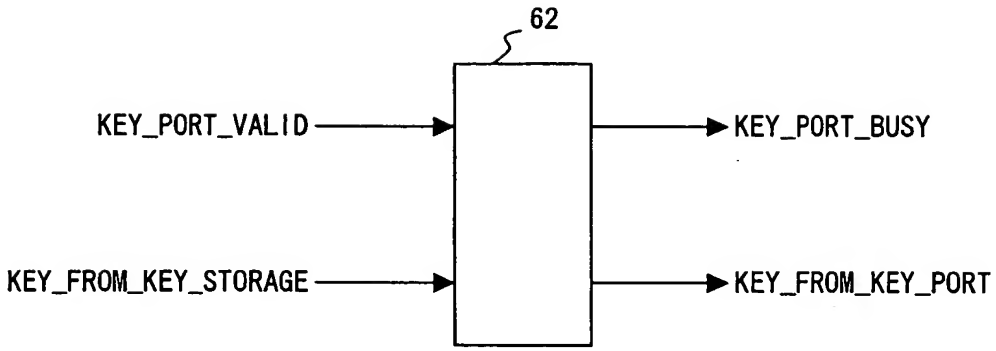


FIG. 8

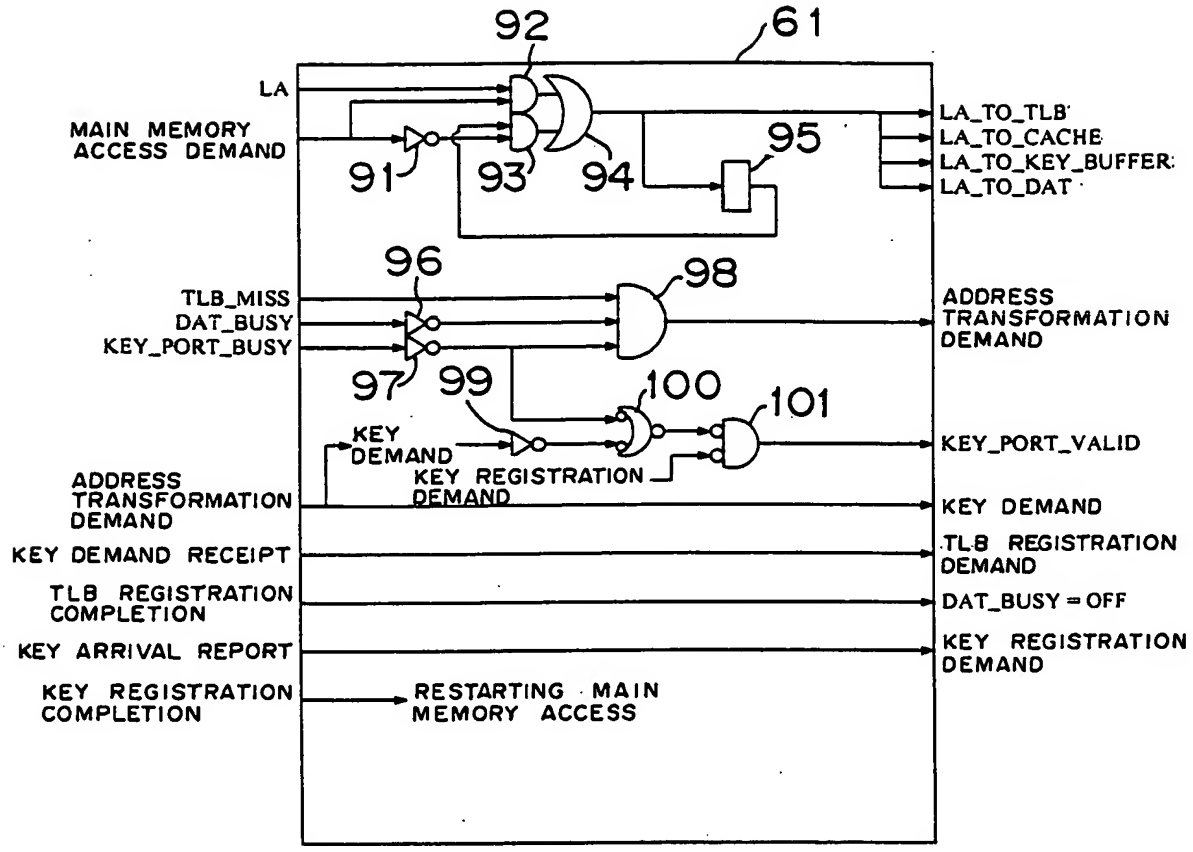

92
61
LA
MAIN MEMORY ACCESS DEMAND
91
93
94
95
LA_TO_TLB
LA_TO_CACHE
LA_TO_KEY_BUFFER
LA_TO_DAT
96
98
TLB_MISS
DAT_BUSY
KEY_PORT_BUSY
97
99
100
101
KEY DEMAND
KEY REGISTRATION DEMAND
KEY_PORT_VALID
ADDRESS TRANSFORMATION DEMAND
ADDRESS TRANSFORMATION DEMAND
KEY DEMAND
KEY DEMAND RECEIPT
TLB REGISTRATION DEMAND
TLB REGISTRATION COMPLETION
DAT_BUSY = OFF
KEY ARRIVAL REPORT
KEY REGISTRATION DEMAND
KEY REGISTRATION COMPLETION
RESTARTING MAIN MEMORY ACCESS

FIG. 9

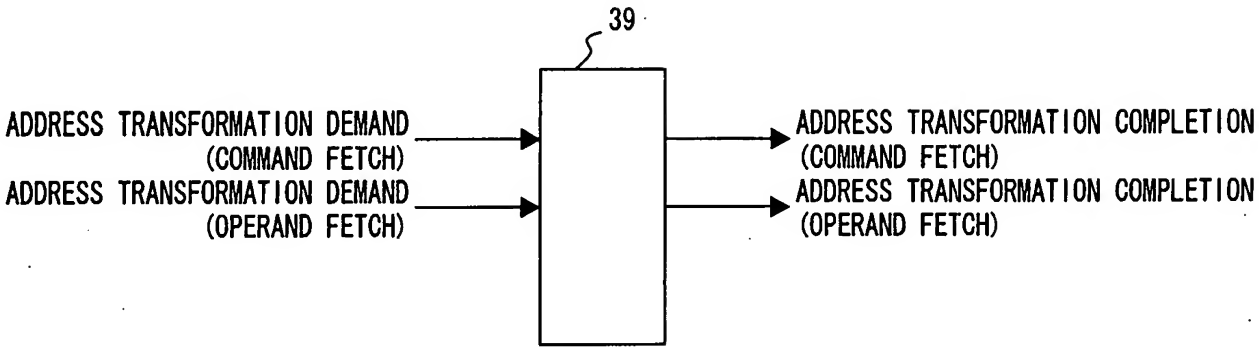

39
ADDRESS TRANSFORMATION DEMAND
(COMMAND FETCH)
ADDRESS TRANSFORMATION DEMAND
(OPERAND FETCH)
ADDRESS TRANSFORMATION COMPLETION
(COMMAND FETCH)
ADDRESS TRANSFORMATION COMPLETION
(OPERAND FETCH)

FIG. 10

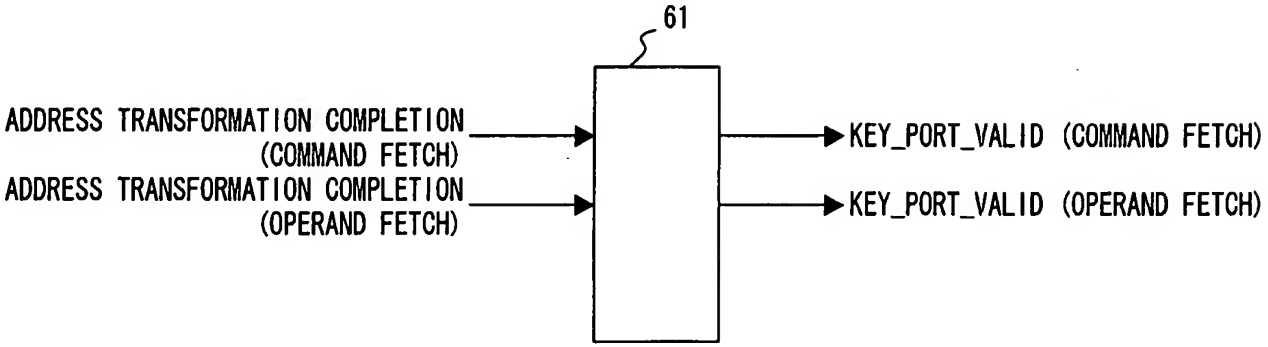

61
ADDRESS TRANSFORMATION COMPLETION (COMMAND FETCH)
ADDRESS TRANSFORMATION COMPLETION (OPERAND FETCH)
KEY_PORT_VALID (COMMAND FETCH)
KEY_PORT_VALID (OPERAND FETCH)

FIG. 11

20220 TSTE80T

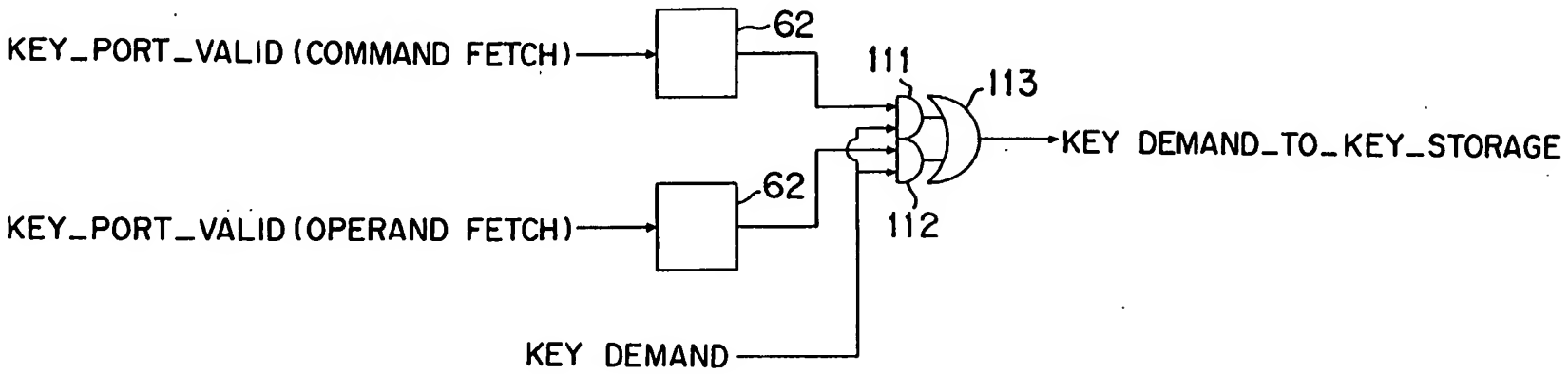


FIG. 12

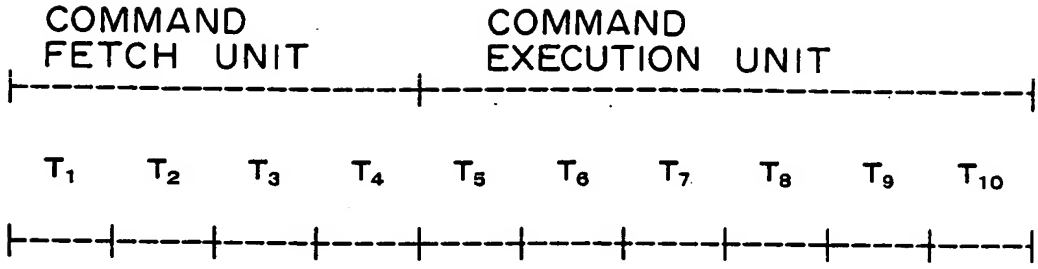

COMMAND
FETCH UNIT
COMMAND
EXECUTION UNIT
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10

FIG. 13

5,758,134

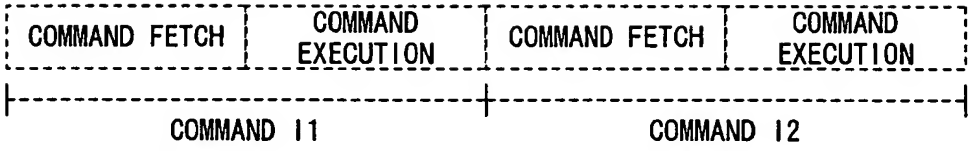


FIG. 14

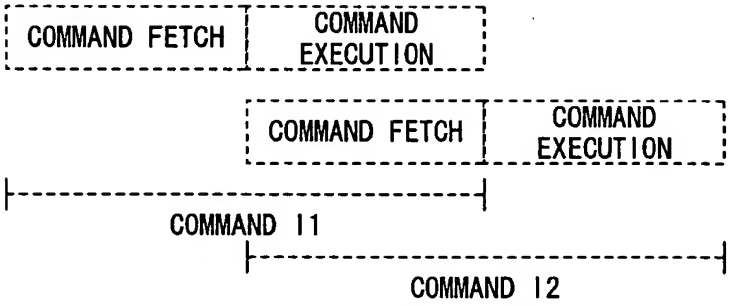
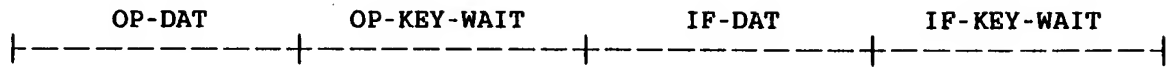

COMMAND FETCH
COMMAND EXECUTION
COMMAND FETCH
COMMAND EXECUTION
COMMAND I1
COMMAND I2

FIG. 15

CONVENTIONAL



PRESENT INVENTION

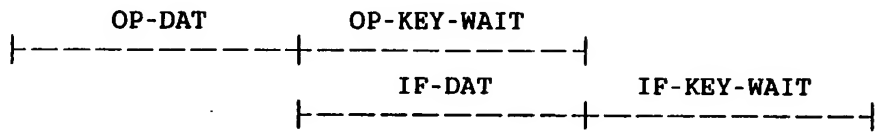
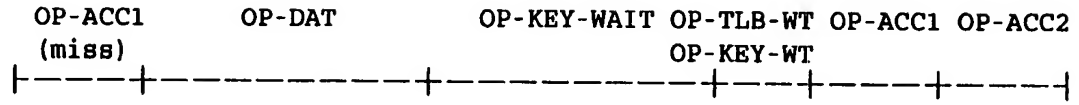


FIG. 16

CONVENTIONAL



PRESENT INVENTION

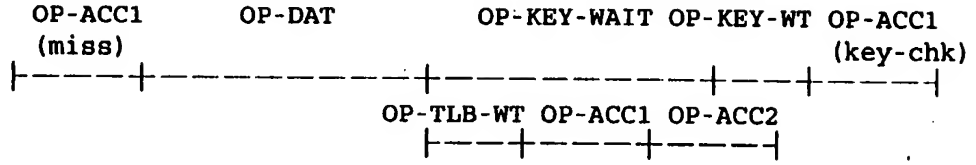


FIG. 17